

Overview

With this project we target the development of reliable safety critication embedded applications, such as used widely in aerospace, in automotive applications, and in medical devices.



We have identified two core issues with the current state of the art

- embedded systems software is normally structured in a way the does not leverage available analysis tools. The software is developed in an analysis-agnostic style that often obfuscates the abstractions made and hampers analyses;
- 2. analysis tools do not leverage available knowledge of the embedded systems' environment. For example, embedded systems software relies critically on specific schedulers that differ significantly from those used on common desktop and mainframe platforms.

Approach

We address the above two core issues by designing and building demonstration *environment* for safety-critical embedded systems software development.

- 1. The first issue is addressed by developing a *new executable* specification language that enforces a code structure that is analysis-friendly. Because scheduling disciplines can have an important influence on both execution and analysis, the language includes a *sublanguage for describing schedulers*.
- 2. The second issue is addressed by building an *analysis tool* that allows direct execution of specifications and also offers verification support based on model checking. The verification algorithms exploit the structure of the code and the schedulers introduced using the specification language. Constraining the analysis to traces that can occur in practice might lead to a significant performance improvement.



SUMMARY

In the past many different methodologies have been developed that support the analysis of software artifacts, and a different set of methodologies have been developed to support software development. We believe that we can gain significant benefits if we combine these two approaches into one methodology that links software development styles directly with existing capabilities of software analysis tools. We apply this methodology to the design and analysis of large complex multi-threaded embedded systems software.



Analysis-aware Design of Embedded Systems Software

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architecture of our framework consists of three ponents: n executive that keeps track of the current state y taking a step corresponding to an action from scheduler that, by looking at the current state, o ctions can be taken next; n analysis tool (e.g. an interpreter or a model ch nonitors the execution, picks an action from thos ne scheduler, and instructs the executive to take orresponding step.	main and updates it the language; decides what necker) that se returned by the
are developing a new specification language that tems implementation language (e.g. C), but has ned semantics, provides higher-level abstraction with formal specifications as part of the source of therface standards and assertion requirements. To close to a typical specification language used i cking (e.g. Promela), but is richer by providing for tract data types.	at is close to a a formally is and allows us ode in the form The language is n model unctions and
specification language is statically typed and proconcurrency and channel-based message passing let used by the language relies on the notions of the transfer and avoids features that can obstitute from the transfer and avoids features that can obstitute and the transfer and avoids features that can obstitute and the transfer and avoids features and unsatises and the transfer and avoids features and unsatises to schedulers.	rovides support ng. The memory f ownership and struct formal fe casts). sed by the d assigning specifying ne language set of enabled
	architecture of our framework consists of three aponents: n executive that keeps track of the current state y taking a step corresponding to an action from scheduler that, by looking at the current state, of ctions can be taken next; n analysis tool (e.g. an interpreter or a model ch nonitors the execution, picks an action from those the scheduler, and instructs the executive to take orresponding step. Decification Language are developing a new specification language that terms implementation language (e.g. C), but has ned semantics, provides higher-level abstraction c interface standards and assertion requirements. To close to a typical specification language used in cking (e.g. Promela), but is richer by providing fut tract data types. process proc(priority : uint, steps : uint sched by PrioSched { function run() { } } specification language is statically typed and pr concurrency and channel-based message passi del used by the language relies on the notions of tership transfer and avoids features that can obs fication attempts (e.g. explicit pointers and unsa specification language also provides features u eduling language: defining process attributes an cesses to schedulers. Cheduling Language are developing a constraint-based language for iron schedulers used in embedded systems. The rates on predefined sets of processes, like the s

[1] M. Florian. A Framework for Systematic Testing of Multi-threaded Applications. Proc. PRDC 2011, to appear. [2] G.J. Holzmann, R. Joshi, and A. Groce. Swarm verification techniques. IEEE Trans. on Software Engineering, accepted for publication, 2011. [3] G.J. Holzmann. Reliable software development: extending the programmer's toolbox. Proc. ETAPS 2011, Saarbrucken, Germany.



Users can define libraries of schedulers, for example those corresponding to the scheduling policies in VxWorks or OSEK, and then reuse them for different applications. ates it The scheduling language is also suitable for specifying nonage; standard constraints that may be used to prioritize a verification hat search or to partition the search space, in an attempt to locate corner cases with potentially anomalous behavior. d by nonpreemptive scheduler PrioSched Next = {p in Enabled | forall p' in Enabled :: priority(p') <= priority(p)}</pre> preemptive scheduler CountSched to a Next = {p in Enabled | forall p' in Enabled :: abs(steps(p) - steps(p')) < 10}</pre> ows us update(steps : uint) { steps = steps + 1 ; } form age is Analysis and Verification Support nd We are developing an interactive development and analysis framework that supports both execution and verification based on model checking of specifications written in the new language. user system spec analyses running in the background pport scheduler emory ip and al The framework exploits the scheduling policies formalized explicitly as part of the design and focuses the analysis on the relevant behaviors. The framework supports the verification of the same Ŋ application under a range of different scheduling policies. The analyses can proceed invisible to the user in the background, using swarm-based verification techniques. **Future Directions** ge bled We want to leverage parallelism that may be ng the available through the use of GPUs and

REFERENCES

multiples execution cores or CPUs.



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