Verification of Analog Circuit Designs via Statistical Model Checking

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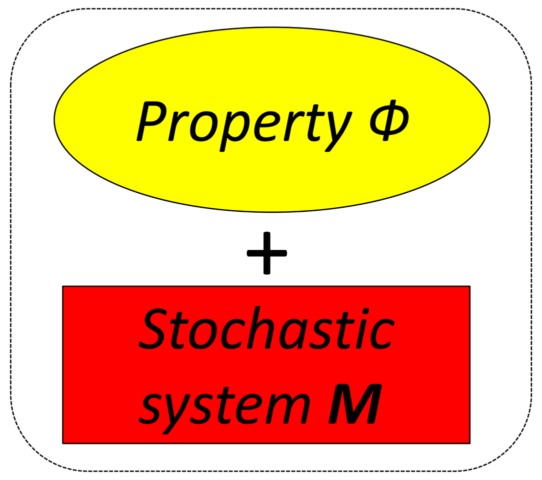
1. Problem

Verification of Analog Circuits with Process Variation

- **Process Variation** brings **uncertainties** into the system
- Model uncertainty with a distribution(**Stochastic systems**)

Verification of Stochastic Systems

- Property specification:
  - a **Property** and a **Probability threshold**
  - "Does **the system fulfill a request within 1.2 ms** with **probability at least .9999**?"
- If Φ = "system fulfills request within 1.2 ms", **decide** between: $P_{\geq .9999}(\Phi)$ or $P_{<.9999}(\Phi)$



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Biased *coin*
Bernoulli random variable of (unknown) parameter p

System satisfies Φ with (unknown) probability p

Question: $P_{\geq\vartheta}(\Phi)$?

2. Bayesian Statistical Model Checking

- Statistical **hypothesis testing**:
  Null hypothesis vs. Alternative hypothesis
  $H_0 : \mathcal{M} \models P_{\geq\theta}(\phi)$ $\quad H_1 : \mathcal{M} \models P_{<\theta}(\phi)$
- Suppose $\mathcal{M}$ satisfies Φ with (unknown) probability p
  - p is given by a random variable (defined on [0,1]) with density *g (*the prior belief that $\mathcal{M}$ satisfies Φ)
- Generate **independent and identically distributed** (iid) sample traces
  - x_i: the i^{th} trace $\sigma_i \models \phi$ ($x_i = 1$ iff $\sigma_i \models \phi$, $x_i = 0$ iff $\sigma_i \not\models \phi$)
  - Then, x_i will be a **Bernoulli trial** with conditional density (**likelihood function**) : $f(x_i|u) = u^{x_i}(1-u)^{1-x_i}$
    - a sample of Bernoulli random variables
  - **Prior probabilities:** $P(H_0)$, $P(H_1) \geq 0$, sum to 1
  - **Posterior probability:** Ratio of Posterior Probabilities

$$P(H_0|X) = \frac{P(X|H_0)P(H_0)}{P(X)}$$

Bayes Theorem, P(X) > 0

$$\frac{P(H_0|X)}{P(H_1|X)} = \frac{P(X|H_0)}{P(X|H_1)} \cdot \frac{P(H_0)}{P(H_1)}$$

Bayes Factor (BF)

- Fix **threshold** T ≥ 1 and $P(H_0)$, $P(H_1)$. **Continue Sampling** until: BF > T: Accept H_0 BF < 1/T: Reject H_0
- ***Theorem** (Error bounds).* When the Bayesian algorithm – using threshold *T* – stops, the following holds:
  Prob ("accept H_0" | H_1) ≤ 1/*T* Prob ("reject H_0" | H_0) ≤ 1/*T*
- ***Theorem** (Termination).* The Sequential Bayesian Statistical MC algorithm **terminates with probability one**.

3. SMC Algorithm

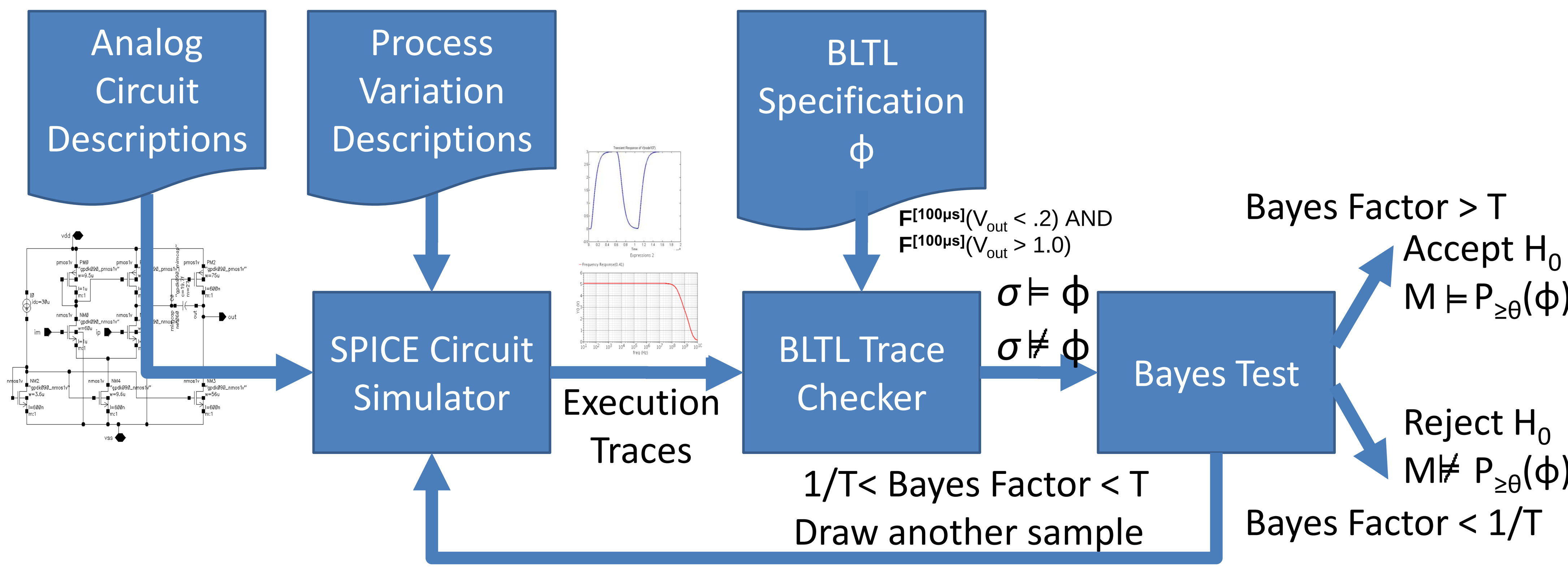
Require: ***Property*** $P_{\geq\vartheta}(\Phi)$***, Threshold*** $T \geq 1$***, Prior density*** *g*
n := 0 {number of traces drawn so far}
x := 0 {number of traces satisfying Φ so far}
repeat
  σ := draw a sample trace from SPICE (iid)
  n := n + 1
  if $\sigma \models \Phi$ **then**
    x := x + 1
  endif
  $\mathcal{B}$ *:= BayesFactor(n, x, ϑ, g)*
until ($\mathcal{B} > T$ ∨ $\mathcal{B} < 1/T$)
if ($\mathcal{B} > T$) **then**
  return "H_0 *accepted*"
else
  return "H_0 *rejected*"
endif

4. Bounded LTL

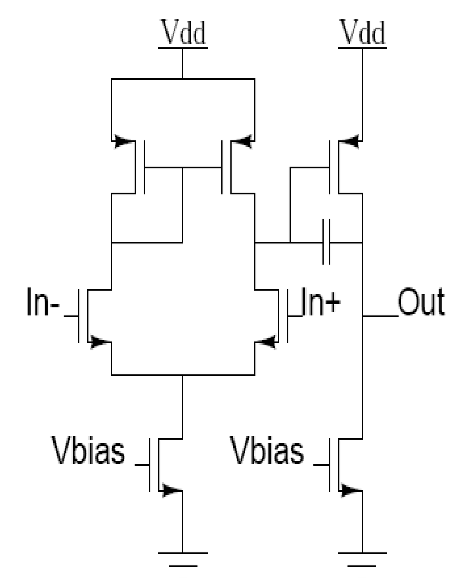
- Extension of Linear Temporal Logic (LTL) with **time bounds** on temporal operators(No ne**X**t operator)
- Let $\sigma = (s_0, t_0), (s_1, t_1), \ldots$ be a trace of the model
  - along states $s_0, s_1, \ldots$, and the system stays in state s_i for time t_i
- **Semantics** of BLTL for trace σ starting at state *k* (σ^k):
  - $\sigma^k \models ap$ iff atomic proposition *ap* true in state s_k
  - $\sigma^k \models \Phi_1$ OR Φ_2 iff $\sigma^k \models \Phi_1$ or $\sigma^k \models \Phi_2$
  - $\sigma^k \models \neg\Phi$ iff $\sigma^k \models \Phi$ does not hold
  - $\sigma^k \models \Phi_1\ \mathcal{U}^t\ \Phi_2$ iff there exists natural *i* s.t
    1) $\sigma^{k+i} \models \Phi_2$
    2) $\Sigma_{j<i}\, t_{k+j} \leq t$
    3) for each $0 \leq j < i$, $\sigma^{k+j} \models \Phi_1$

    "within time *t*, Φ_2 will be true and Φ_1 will hold until then"
- Online monitoring
  - Monitor the trace as it is generated, need not store the trace
  - Enable Monitoring for long traces
- Modify the model checking algorithm for alternation-free mu-calculus, to make it online
  - A DAG data structure
    - Created from the parsing tree of *Φ*
    - Online monitored values propagated from the leaves
    - Optimized by merging similar sub-trees and some bookkeeping
    - Algorithm terminates when the root is evaluated

5. Tool Overview



6. Experimental Results



A simple example: an Op amp with typical specifications

Specifications			BLTL Specifications
1	Input Offset Voltage	< 1 mV	$\mathbf{F}^{[100\mu s]}(V_{out} = .6)$ AND $\mathbf{G}^{[100\mu s]}((V_{out} = .6) \rightarrow (\lvert V_{in+} - V_{in-}\rvert < .001))$
2	Output Swing Range	.2 V to 1.0 V	$\mathbf{F}^{[100\mu s]}(V_{out} < .2)$ AND $\mathbf{F}^{[100\mu s]}(V_{out} > 1.0)$
3	Slew Rate	> 25 V/μSec	$\mathbf{G}^{[100\mu s]}(((V_{out} > 1.0 \text{ AND } V_{in} > .65) \rightarrow \mathbf{F}^{[0.032\mu s]}(V_{out} < .2))$ AND $(V_{out} < .2 \text{ AND } V_{in} < .55) \rightarrow \mathbf{F}^{[0.032\mu s]}(V_{out} < 1.0))$
4	Open-Loop Voltage Gain	> 8000 V/V	$\mathbf{G}^{[1KHz]}(V\ mag_{out} > 8000)$
5	Loop-Gain Unit-gain Frequency	> 10 MHz	$\mathbf{G}^{[10MHz]}(V\ mag_{out} > 1)$
6	Phase Margin	> 60°	$\mathbf{F}^{[10GHz]}(V\ mag_{out} = 1)$ AND $\mathbf{G}^{[10GHz]}((V\ mag_{out} = 1) \rightarrow (Vphase_{out} > 60°))$

Comparison of different probability threshold
T = 1000 (probability of error < .001)
θ = ranged from .7 to .999
SMC testing result: reject / accept null hypothesis

Samples/Runtime					
Probability threshold θ					
Spec	.7	.8	.9	.99	.999
1	77/105s	9933/12161s	201/275s	10/13s	7/9s
2	16/18s	24/27s	44/51s	239/280s	693/813s
3	16/23s	24/31s	44/57s	239/316s	693/916s
4	23/26s	43/49s	98/114s	1103/1309s	50/57s
5	16/18s	24/28s	44/51s	239/279s	693/807s
6	16/20s	24/30s	44/55s	239/303s	693/882s

- In most configurations, SMC terminates with sample sizes less than 1000.
- When θ is close to the actual probability of model satisfying the property, SMC needs more samples to draw the conclusion.

Comparison of SMC and 1000-sample Monte Carlo
T = 1000 (probability of error < .001)
θ = 0.95 (typical target yield for the design)
Monte Carlo analysis : not satisfy /satisfy yield
SMC testing result : reject / accept null hypothesis

Monte Carlo (1000 samples) — Measured Value					SMC
Specifications		Mean	Stddev	Yield	Sample/Runtime
1	Input Offset Voltage (V)	.436	.597	.826	31/39s
2	Swing Range Min (V)	.104	.006	1.00	77/98s
	Swing Range Max (V)	1.08	.005	1.00	77/98s
3	Negative Slew Rate (V/μSec)	-40.2	1.17	1.00	77/98s
	Positive Slew Rate (V/μSec)	56.4	2.54	1.00	77/98s
4	Open-Loop Voltage Gain (V/V)	8768.	448	.975	239/303s
5	Loop-Gain UGF (MHz)	19.9	.30	1.00	77/98s
6	Phase Margin (°)	64.1	.44	1.00	77/98s

- Interpretation of Monte Carlo Result by 3-sigma performances: Spec 1, 4 not satisfied, need more design margins
- SMC needs fewer samples in most cases (about ¼)
  The sample size is determined by the test strength needed

7. Discussion and Conclusion

- The Bayesian SMC algorithm is faster when
  - θ is away from the unknown probability p
  - θ is close to 1 (or 0): the variance of a Bernoulli random variable is the largest at p = 0.5
  - Suitable for circuit verification: circuits are designed to have high yields (yields close to 1)
- The Bayesian SMC can be easily integrated in the current analog validation flow because it relies only on Monte Carlo sampling and SPICE simulation.

8. Future Work

- More experiments
  - Larger examples
  - More complex specifications
- Fully integrated with SPICE simulator
- Introduce the idea of Importance sampling